Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) An output buffer configured for use within DRAM applications, said output buffer comprising:

an output driver circuit configured for providing an output signal for said output buffer; and

a slew rate control circuit coupled to said output driver circuit and configured for receiving a drive input signal and for controlling a slew rate of said drive input signal based on a level of voltage provided from a power supply to said output driver circuit, wherein increases in said level of voltage decrease said slew rate and decreases in said level of voltage increase said slew rate.

2. (Original) The output buffer according to claim 1, wherein said output buffer further comprises a predriver circuit configured for providing said drive input signal.

3. (Original) The output buffer according to claim 2, wherein said output buffer is coupled between said predriver circuit and said output driver circuit.

4. (Original) The output buffer according to claim 1, wherein said predriver circuit comprises:

a pull-up predriver circuit for providing a pull-up input signal for controlling said pull-up transistor of said output driver circuit; and

a pull-down predriver circuit for providing a pull-down input signal for controlling said pull-down transistor of said output driver circuit.

5. (Currently amended) The output buffer according to claim 1, wherein said output driver circuit comprises:

a pull-up transistor having an input terminal ~~configured for coupling~~ connected to the power supply, and a control terminal coupled to said slew rate control circuit; and

a pull-down transistor having an input terminal ~~configured for coupling~~ connected to a ground connection, an output terminal coupled to an output terminal of said pull-up transistor, and a control terminal coupled to said slew rate control circuit.

6. (Original) The output buffer according to claim 1, wherein said slew rate control circuit comprises:

a first amplifier circuit configured for controlling a slew rate of a pull-up input signal and providing said controlled pull-up input signal to said output driver circuit; and

a second amplifier circuit configured for controlling a slew rate of a pull-down input signal and providing said controlled pull-down input signal to said output driver circuit.

7. (Currently amended) An output buffer configured for use in memory applications, said output buffer comprising:

an output driver circuit configured for providing an output signal for said output buffer, wherein said output driver circuit comprises:

a pull-up transistor having an input terminal ~~configured for coupling~~ connected to a power supply; and

a pull-down transistor having an input terminal ~~configured for coupling~~ connected to a ground connection, an output terminal coupled to an output terminal of said pull-up transistor; and

a slew rate control circuit coupled to control terminals of said pull-up transistor and said pull-down transistor of said output driver circuit and configured for controlling a slew rate of a drive input signal.

8. (Currently amended) The output buffer according to claim 7, wherein said slew rate control circuit is configured for controlling a slew rate of a drive input signal based on a level of voltage in said power supply provided to said output driver circuit, wherein increases in said level of voltage decrease said slew rate and decreases in said level of voltage increase said slew rate.

9. (Original) The output buffer according to claim 7, wherein said slew rate control circuit comprises a first amplifier circuit configured for controlling a slew rate of a pull-up input signal and providing said controlled pull-up input signal to said output driver circuit; and

a second amplifier circuit configured for controlling a slew rate of a pull-down input signal and providing said controlled pull-down input signal to said output driver circuit.

10. (Original) The output buffer according to claim 7, wherein said output buffer further comprises a predriver circuit configured for providing said drive input signal.

11. (Original) The output buffer according to claim 10, wherein said predriver circuit is configured for providing a pull-up input signal for controlling said pull-up transistor of said output driver circuit, and for providing a pull-down input signal for controlling said pull-down transistor of said output driver circuit.

12. (Original) The output buffer according to claim 11, wherein said predriver circuit comprises:

a pull-up predriver circuit for providing said pull-up input signal for controlling said pull-up transistor of said output driver circuit; and

a pull-down predriver circuit for providing said pull-down input signal for controlling said pull-down transistor of said output driver circuit.

13. (Original) An output buffer configured for use within DRAM applications, said output buffer comprising:

a predriver circuit configured for providing a drive input signal; and

a slew rate control circuit coupled to said predriver circuit and configured for controlling a slew rate of said drive input signal based on a level of voltage in a power supply, wherein said slew rate control circuit comprises:

a first amplifier circuit configured for controlling a slew rate of a pull-up input signal; and

a second amplifier circuit configured for controlling a slew rate of a pull-down input signal.

14. (Original) The output buffer according to claim 13, wherein said output buffer further comprises an output driver circuit configured for providing an output signal for said output buffer.

15. (Original) The output buffer according to claim 14, wherein said output driver circuit is configured for receiving said level of voltage from the power supply.

16. (Original) The output buffer according to claim 14, wherein said output driver circuit is configured to receive a control signal from said slew rate control circuit.

17. (Original) The output buffer according to claim 14, wherein said slew rate control circuit comprises:

a first amplifier circuit is configured providing said controlled pull-up input signal to said output driver circuit; and

a second amplifier circuit configured for providing said controlled pull-down input signal to said output driver circuit.

18. (Original) The output buffer according to claim 13, wherein said first amplifier circuit comprises a first operational transconductance amplifier, and said second amplifier circuit comprises a second operational transconductance amplifier.

19. (Original) The output buffer according to claim 13, wherein said first amplifier circuit is configured with a first voltage-controlled current source, and said second amplifier circuit is configured with a second voltage-controlled current source.

20. (Original) The output buffer according to claim 19, wherein said first voltage-controlled current source and said second voltage-controlled current source are configured for controlling biasing current for said first amplifier circuit and said second amplifier circuit based on voltage changes of the power supply.

21. (Original) The output buffer according to claim 19, wherein said first voltage-controlled current source and said second voltage-controlled current source are configured for receiving a voltage signal representative of voltage in the power supply and for comparison of said representative voltage signal to a reference voltage signal.

22. (Original) The output buffer according to claim 19, wherein at least one of said first voltage-controlled current source and said second voltage-controlled current source comprises:

a differential pair of transistors comprising a first transistor and a second transistor, said first transistor having a control terminal coupled to said representative voltage signal and an output terminal coupled to the power supply, said second transistor having a control terminal coupled to said reference voltage signal and an output terminal coupled to an input terminal of said first transistor;

a first fixed current source coupled to said input terminals of said first transistor and said second transistor;

a third transistor having an output terminal coupled to an output terminal of said second transistor and further coupled to one of said first amplifier circuit and said second amplifier circuit, and a control terminal coupled to said reference voltage signal; and

a second fixed current source coupled to an output terminal of said third transistor.

23. (Original) The output buffer according to claim 22, wherein said output buffer further comprises a supply voltage generation circuit for generating a said representative voltage signal, said supply voltage generation circuit coupled to said at least one of said first voltage-controlled current source and said second voltage-controlled current source.

24. (Original) A slew rate control circuit for controlling the slew rate of an output signal of an output buffer, said slew rate control circuit comprising:

a first amplifier circuit for receiving a first input drive signal and controlling a slew rate of said first input drive signal based on changes in voltage of a power supply coupled to the output buffer; and

a second amplifier circuit for receiving a second input drive signal and controlling a slew rate in said second input drive signal based on changes in voltage of the power supply coupled to the output buffer.

25. (Original) The slew rate control circuit according to claim 24, wherein said slew rate control circuit further comprises:

a first current source coupled to said first amplifier circuit, said first current source configured for providing a first biasing current to said first amplifier circuit to facilitate control of said slew rate of said first input drive signal; and

a second current source coupled to said second amplifier circuit, said second current source configured for providing a second biasing current to said second amplifier circuit to facilitate control of said slew rate of said second input drive signal.

26. (Original) The slew rate control circuit according to claim 25, wherein said first current source is configured to adjust said first biasing current based on a level of voltage in the power supply to facilitate control of the slew rate of the output signal of the output buffer.

27. (Original) The slew rate control circuit according to claim 25, wherein said first current source is configured to decrease said first biasing current when said level of voltage in the power supply increases, and to increase said first biasing current when said level of voltage in the power supply decreases, to facilitate control of the slew rate of the output signal of the output buffer.

28. (Original) The slew rate control circuit according to claim 25, wherein said second current source is configured to decrease said second biasing current when said level of voltage in the power supply increases, and to increase said second biasing current when said level of voltage in the power supply decreases, to facilitate control of the slew rate of the output signal of the output buffer.

29. (Original) The slew rate control circuit according to claim 25, wherein said first current source is configured to compare a voltage signal representative of voltage in the power supply with a reference voltage signal to determine whether to adjust said first biasing current.

30. (Original) The slew rate control circuit according to claim 24, wherein said first amplifier circuit comprises a first operational transconductance amplifier and said second amplifier circuit comprises a second operational transconductance amplifier.

31. (Original) The slew rate control circuit according to claim 25, wherein said first current source comprises a first voltage-controlled current source and said second current source comprises a second voltage-controlled current source.

32. (Original) The slew rate control circuit according to claim 24, wherein at least one of said first amplifier circuit and said second amplifier circuit comprises a first differential pair input circuit and a second differential pair input circuit.

33. (Original) The slew rate control circuit according to claim 32, wherein said first differential pair input circuit and said second differential pair input circuit are configured to provide differential input terminals to said at least one of said first amplifier circuit and said second amplifier circuit.

34. (Original) The slew rate control circuit according to claim 32, wherein said first differential pair input circuit comprises a p-channel differential input pair of transistors and said second differential pair input circuit comprises an n-channel differential input pair of transistors.

35. (Original) The slew rate control circuit according to claim 32, wherein said first differential pair input circuit is coupled to a voltage-controlled current source and said second differential pair input circuit is coupled to another voltage-controlled current source.

36. (Original) The slew rate control circuit according to claim 24, wherein said first amplifier circuit comprises a first output stage circuit, and said second amplifier circuit comprises a second output stage circuit.

37. (Original) The slew rate control circuit according to claim 25, wherein at least one of said first current source and said second current source comprises:

a differential pair of transistors comprising a first transistor and a second transistor, said first transistor coupled to said representative voltage signal and to the power supply, said second transistor coupled to said reference voltage signal;

a first fixed current source coupled to an output of said first transistor and said second transistor;

a third transistor coupled to said second transistor and to one of said first operational transconductance amplifier and said second operational transconductance amplifier, and further coupled to said reference voltage signal; and

a second fixed current source coupled to a said third transistor.

38. (Original) The slew rate control circuit according to claim 37, wherein at least one of said first current source and said second current source comprises:

a first fixed current source coupled to an output of said first transistor and said second transistor; and

a second fixed current source coupled to a said third transistor.

39. (Original) A method for slew rate regulation of an output signal in an output buffer, said method comprising:

determining a level of voltage of a power supply for said output buffer; and

controlling said slew rate of said output signal through adjustment of a slew rate of an input drive signal based on said level of voltage of the power supply.

40. (Original) The method according to claim 39, wherein said method further comprises receiving in a slew rate control circuit said input drive signal from a predriver circuit.

41. (Original) The method according to claim 39, wherein said method further comprises comparing said level of voltage of said power supply with a reference voltage.

42. (Original) A method for slew rate regulation of an output signal in an output buffer, said method comprising:

receiving in a slew rate control circuit an input drive signal;

comparing a level of voltage of a power supply with a reference voltage; and

controlling said slew rate of the output signal through adjustment of a slew rate of said input drive signal based on said level of voltage of the power supply.

43. (Original) The method according to claim 42, wherein said comparing said level of voltage of the power supply with said reference voltage is conducted within a voltage-controlled current source.

44. (Original) A method for slew rate regulation of an output signal in an output buffer, said method comprising:

controlling with a slew rate control circuit a slew rate of the output signal through adjustment of a slew rate of an input drive signal based on a level of voltage of a power supply through at least one of:

increasing a bias current in an amplifier circuit of said slew rate control circuit when said level of voltage of the power supply is less than a reference voltage; and

decreasing a bias current in an amplifier circuit of said slew rate control circuit when said level of voltage of the power supply is greater than a reference voltage.

45. (Original) The method according to claim 44, wherein said method further comprises:

receiving in said slew rate control circuit said input drive signal from a predriver circuit;

determining a level of voltage of said power supply for the output buffer.

46. (Original) The method according to claim 44, wherein said step of determining said level of voltage of said power supply comprises scaling down voltage of said power supply to provide said level of voltage.

47. (Original) The method according to claim 44, wherein said step of controlling said slew rate comprises adjustment of a slew rate in at least one of a pull-up drive signal and a pull-down drive signal.

48. (Original) A DRAM output buffer comprising:

a predriver circuit configured for providing at least one of a pull-up input signal and a pull-down input signal; and

a slew rate control circuit configured for controlling a slew rate of at least one of said pull-up input signal and said pull-down input signal based on levels of voltage of a power supply coupled to said output driver circuit, and configured for providing at least one of a controlled pull-up signal and a controlled pull-down signal.

49. (Original) The DRAM output buffer according to claim 48, wherein said DRAM output buffer further comprises an output driver circuit configured for receiving at least one of said controlled pull-up signal and said controlled pull-down signal and for providing an output signal.

50. (Original) The DRAM output buffer according to claim 48, wherein said slew rate control circuit comprises:

a first amplifier circuit for receiving said pull-up input signal and controlling a slew rate of said pull-up input signal based on changes in voltage of a power supply; and

a second amplifier circuit for receiving said pull-down input signal and controlling a slew rate in said pull-down input signal based on changes in voltage of the power supply.

51. (Original) The DRAM output buffer according to claim 48, wherein said DRAM output buffer further comprises an output buffer coupled to a power supply, and said slew rate control circuit comprises:

a first amplifier circuit for receiving said pull-up input signal and controlling a slew rate of said pull-up input signal based on changes in voltage of the power supply coupled to the output buffer;

a first current source coupled to said first amplifier circuit, said first current source configured for providing a first biasing current to said first amplifier circuit to facilitate control of said slew rate of said pull-up input signal;

a second amplifier circuit for receiving said pull-down input signal and controlling a slew rate in said pull-down input signal based on changes in voltage of the power supply coupled to the output buffer; and

a second current source coupled to said second amplifier circuit, said second current source configured for providing a second biasing current to said second amplifier circuit to facilitate control of said slew rate of said pull-down input signal.

52. (Original) A memory system having an output buffer configured for providing an operating voltage to a memory device, said output buffer comprising:

a slew rate control circuit configured for receiving at least one input control signal and for controlling a slew rate of a controlled drive signal based on voltage changes in a power supply, said slew rate control circuit comprising a first amplifier circuit for receiving a pull-up input signal, and a second amplifier circuit for receiving a pull-down input signal.

53. (Original) The memory system according to claim 52, wherein said output buffer further comprises:

a predriver circuit configured for providing at least one of said pull-up input signal to said first amplifier circuit and said pull-down input signal to said second amplifier circuit.

54. (Original) The memory system according to claim 52, wherein said output buffer further comprises an output driver circuit configured for providing an output signal, said output driver circuit coupled to the power supply.

55. (Original) The memory system according to claim 37, wherein said slew rate control circuit comprises:

a first current source coupled to said first amplifier circuit, said first current source configured for providing a first biasing current to said first amplifier circuit to facilitate control of said slew rate of said pull-up input signal; and

a second current source coupled to said second amplifier circuit, said second current source configured for providing a second biasing current to said second amplifier circuit to facilitate control of said slew rate of said pull-down input signal.

56. (Original) An electronic system comprising a processor, a supply and a memory system, said memory system having an output buffer comprising:

an output driver circuit configured for providing an output signal for said output buffer; and

a slew rate control circuit configured to receive a drive input signal and to provide a controlled drive signal to said output driver circuit, said slew rate control circuit configured for controlling a slew rate for said controlled drive signal based on voltage level in a power supply coupled to said output driver circuit.

57. (Original) The electronic system according to claim 56, wherein said output buffer further comprises a predriver circuit configured for providing said drive input signal, and said slew rate control circuit comprises:

an amplifier circuit for receiving said drive input signal and controlling said slew rate of said controlled drive signal based on said voltage level of the power supply; and

a current source configured with said amplifier circuit, said current source configured for providing a biasing current to said amplifier circuit to facilitate control of said slew rate of said controlled drive signal through decreases and increases in said biasing current based on increases and decreases in said voltage level of the power supply.

58. (Original) A slew rate control circuit for controlling the slew rate of an output signal of an output buffer, said slew rate control circuit comprising:

an amplifier circuit for receiving an input drive signal and controlling a slew rate of said input drive signal based on a level of voltage of a power supply coupled to the output buffer; and

a current source coupled to said amplifier circuit, said current source configured for providing a biasing current to said amplifier circuit to facilitate control of said slew rate of said input drive signal.

59. (Original) The slew rate control circuit according to claim 58, wherein said slew rate control circuit is configured to control any increases and decreases in the slew rate of the output signal of the output buffer through decreases and increases in said biasing current.